Amendments to the Claims:

1. Apparatus comprising:

first and second data input/output circuits, each of said circuits receiving data output from the other and releasing data stored therein; and

a data bus transferring data between said first and second data input/output circuits,

wherein, upon data output being successively switched from said first data input/output circuit to said second data input/output circuit, said second data input/output circuit takes in data output from said first data input/output circuit and releases said data taken thereinto to said data bus.

2 (Currently amended). Apparatus according to claim 1, wherein after said second data input/output circuit outputs said data taken thereinto to said data bus, said second data input/output circuit outputs ~~said~~ data thereof to said data bus.

3. Apparatus according to claim 1, wherein each of said first and second data input/output circuits includes:

an output buffer for outputting data thereof;

an input buffer for receiving data from the other data input/output circuit; and

a relay line joining said buffers for transferring said data to said output buffer, said data being output from the other data input/output circuit and being received by said input buffer.

4. Apparatus according to claim 3, wherein said output buffer outputs said data to said data bus, said data being output from the other data input/output circuit and being transferred from said relay line.

5 (Currently amended). Apparatus comprising:

a memory controller for issuing a data read/write instruction;

a memory for executing a data read/write operation in response to the data read/write instruction from said memory controller; and

a bus for connecting said memory controller and said memory,

wherein said memory controller includes:

a first output buffer for outputting write data to said bus, said write data being written to said memory;

a first input buffer for receiving read data via said bus, said read data being read out from said memory;

a first output line for transferring said write data to said first output buffer;

a first input line for transferring said read data received by said first input buffer;

a first multiplexer arranged on said first output line; and

a first relay line connecting said first input line and said first multiplexer, and further wherein

said memory includes:

a memory cell for storing read/write data;

a second output buffer for outputting said read data to said bus, said read data being read out from said memory cell in response to ~~said~~ a read instruction of said memory controller;

a second input buffer for receiving said write data output from said first output buffer of said memory controller;

a second output line for transferring said read data to said second output buffer, said read data being transferred from said memory cell;

a second input line for transferring said write data received by said second input buffer to said memory cell;

a second multiplexer arranged on said second output line; and

a second relay line for connecting said second input line and said second multiplexer.

6. Apparatus according to claim 5, wherein when said memory controller issues the read instruction to said memory, said memory selects said second output line by said second multiplexer thereof and reads out said read data from said memory cell to output said read data to said bus via said second output line and said second output buffer, and said memory controller receives said read data via said bus by said first input buffer thereof, and selects said first relay line by said first multiplexer thereof after passage of a predetermined time to output said read data to said bus via said first input line, said first relay line, said first output line and said first output buffer.

7. Apparatus according to claim 6, wherein said memory controller outputs said read data to said bus, and then takes in said read data from said bus.

8 (Currently amended). Apparatus according to claim 5, wherein, when said memory controller issues ~~the~~ a write instruction to said memory, said memory controller selects said first output line by said first multiplexer thereof and outputs said write data to said bus via said first output line and said first output buffer, ~~said write data being transferred from the outside,~~ and said memory receives said write data via said bus by said second input buffer thereof, and selects said second relay line after passage of a predetermined time by said second multiplexer thereof to output said write data to said bus via said second input line, said second relay line, said second output line and said second output buffer.

9. Apparatus according to claim 8, wherein said memory outputs said write data to said bus, and then takes in said write data from said bus.

10 (Currently amended). Apparatus according to claim 5, wherein, when said memory controller issues the data read/write instruction to said memory successively, said memory selects said second output line by said second multiplexer thereof, and reads out said read data from said memory cell to output said read data to said bus via said second output line and said second output buffer, said memory controller receives said read data via said bus by said first input buffer thereof, and selects said first relay line after passage of a predetermined time by said first multiplexer thereof to output said read data to said bus via said first input line, said first relay line, said first output line and said first output buffer, said memory controller selects said first output line by said first multiplexer thereof, and outputs said write data to said bus via said first output line and said first output buffer, ~~said write data being transferred from the outside,~~ and said memory receives said write data via said bus by said second input buffer thereof, and selects said second relay line after passage of a predetermined time by said second multiplexer thereof to output said write data to said bus via said second input line, said second relay line, said second output line and said second output buffer.

11 (Currently amended). Apparatus comprising:

an input/output cell in which a first buffer for outputting output data to a data bus and a second buffer for receiving input data transferred from said data bus are connected to said data bus;

a data holding circuit for holding said output data and said input data;

an output line for transferring said output data held in said data holding circuit to said first buffer;

an input line for transferring said input data received by said second buffer to said data holding circuit;

a relay line for transferring said input data to said ~~output~~ first buffer via said second buffer; and

a line selection circuit for selectively making any of data transfers of said output line and said relay line valid.

12 (Currently amended). Apparatus according to claim 11, ~~wherein the data input/output circuit further comprises:~~ further comprising:

a control signal generating circuit for outputting an output control signal to said input/output cell, the output control signal being for controlling whether said data can be output from said input/output cell.

13. Apparatus according to claim 12, wherein said control signal generating circuit outputs a selection signal to said line selection circuit, said selection signal being for controlling selection in said line selection circuit.

14. Apparatus according to claim 13, wherein, while said control signal generating circuit is outputting said selection signal to said line selection circuit, said input data received by said second buffer is output to said data bus via said relay line and said first buffer.

15. Apparatus according to claim 14, wherein said control signal generating circuit outputs an output control signal to said input/output cell, said output control signal enabling said input/output cell to output the data; and said control signal generating circuit outputs said selection signal to said line selection circuit after passage of a predetermined time from the outputting of said output control signal, said selection signal being for selecting said relay line.

16 (Currently amended). A method comprising the steps of:

outputting a first signal to a bus from ~~said~~ a first input/output circuit, said first signal being data of said first data input/output circuit;

taking in said first signal from said bus by ~~said~~ a second data input/output circuit; and

outputting said first signal to said bus by said second data input/output circuit.

17. The method according to claim 16, further comprising the step of:

outputting a second signal to said bus by said second data input/output circuit, the second signal being data of said second data input/output circuit, after said second data input/output circuit outputs said first signal to said bus.

18. The method according to claim 17, further comprising the steps of:

taking in said second signal from said bus by said first data input/output circuit after said second data input/output circuit outputs said second signal to said bus; and

outputting said second signal to said bus by said first data input/output circuit.